Vaibhav Krishna Garimella

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EDUCATION

Columbia University New York, NY
MS in Electrical Engineering Expected Dec 2026
Coursework: Advances in VLSI Design Automation, Advanced Logic Design, SoC Platforms, Formal Verification

Indian Institute of Technology Madras Chennai, IN
BTech in Engineering Physics, GPA: ***8.8/10*** Jul 2025
Coursework: Embedded Memory Design, Digital IC Design, Analog IC Design, Neuromorphic Computing, Deep Learning for Imaging, Mapping DSP Algos. to Arch., Computer Organization, Machine Learning Techniques

ACADEMIC EXPERIENCE

Compute In-Memory Group @ IIT Madras Chennai, IN
Hybrid-Domain Compute In-Memory ***Chip Tape-Out*** Aug 2024 - Aug 2025

- Designed layout for the full SRAM array (~40KB) and peripherals like Sense Amp and Word Line Drivers and performed RC-extracted Monte Carlo simulations across corners to verify functionality and compute read/write times
- Designed a tunable Voltage-to-Time Converter (VTC) for different MAC range inputs for charge domain operation
- Analyzed layer-wise statistics of various Neural Networks based on ADC-bit and MAC length limitations while maintaining an accuracy drop of less than 0.1% from software baseline

Shakti Processor Chennai, IN
Instruction Set Architecture Implementation and Testing (Github) Dec 2023 - Jun 2024

- Implemented Packed Single Instruction, Multiple Data (PSIMD) instructions on the C-class SoC in BlueSpecVerilog
- Benchmarked area and speed metrics against existing M-extension instructions using Synopsys Design Compiler

Team Avishkar Hyperloop Chennai, IN
PCB Design for Inverter Control (Github) Sep 2022 - Jul 2023

- Designed and tested a 4-layer PCB to run the inverter and collect pod-critical data from the Intelligent Power Module
- Configured a Battery Management System (BMS) with self-designed high voltage battery packs, tested CAN communication and implemented fault states through the BMS based on safety limits

COURSE PROJECTS

Charge Domain Compute In-Memory Engine [Embedded Memory Design] IIT Madras

- Designed a Charge-Domain 9T-1C compute-cell based Compute In-Memory engine for MNIST image classification
- Performed Monte-Carlo simulations to verify functionality of memory and compute columns

NVM based Compute In-Memory Engine [Neuromorphic Computing] *(Github)* IIT Madras

- Built a 2-layer feedforward neural network using CMOS neurons and NVM (RRAMs and FeFETs) synaptic arrays
- Performed hardware-aware training to account for binarization of first layer outputs, inherently incorporating a squeezing function as part of the inference

8-bit Carry Save Multiplier [Digital IC Design] IIT Madras

- Designed a transistor-level schematic and layout of an 8-bit Carry Save Multiplier with multi-level Carry Lookahead Adder for a more optimized vector merge
- Pipelined the schematic using C2MOS Flip Flops to achieve an 85% increase in clock frequency to 3.75MHz

Fully Differential Inverting Amplifier Design [Analog IC Design] IIT Madras

- Designed a fully differential op-amp with a closed loop DC gain of 15.54dB and a 3dB bandwidth of 16.04MHz
- Implemented the op-amp with two-stage common-mode feedback to achieve an open loop gain of 70.29dB

SKILLS

Programming Languages: Verilog, Python, C, C++, Tcl, MATLAB
Tools and Frameworks: Cadence Virtuoso, Genus, Innovus, Synopsys Design Compiler, Vivado, ADS, Altium Designer
General: Git, Vim, Linux, Bash, MakeFile

ACHIEVEMENTS

• JN Tata Endowment Scholar • JEE Advanced [All India Rank 1013] • KVPY SA Scholar [All India Rank 365]